CLAIMS

What is claimed is:

1. A computer implemented process for electronic design automation, said process comprising the steps of:

receiving an HDL description of an integrated circuit design;

generating a scannable netlist based on said HDL description, said scannable netlist comprising a scan chain;

partitioning said scan chain into a plurality of sets of re-orderable scan cells, wherein partitioning information which describes the scan cells of each set is generated; and

based on said partitioning information, re-ordering scan cells of said scan chain during layout processes of said integrated circuit design, said step of re-ordering only re-ordering scan cells of a same set and not re-ordering scan cells of different sets.

2. The computer implemented process as recited in Claim 1 wherein said step of partitioning further comprises the step of grouping scan cells of said scan chain into different sets based on their respective clock domains.

3. The computer implemented process as recited in Claim 1 wherein said step of partitioning further comprises the step of grouping scan cells of said scan chain into different sets based on their respective edge sensitivity types.

4. The computer implemented process as recited in Claim 1 wherein said step of partitioning further comprises the step of grouping scan cells of said scan chain into different sets based on their respective positions in relation to a reconfigurable multiplexer of said scan chain.

5. The computer implemented process as recited in Claim 1 wherein said step of partitioning further comprises the step of grouping scan cells of said scan chain into different sets based on their respective clock skew tolerance levels.

6. The computer implemented process as recited in Claim 1 wherein said step of partitioning further comprises the step of grouping scan cells of said scan chain into different sets based on their respective surrounding cone logic.

7. The computer implemented process as recited in Claim 1 wherein said step of partitioning further comprises the step of grouping scan cells of said scan chain into different sets based on their respective output switching times.

8. A computer controlled electronic design automation system comprising:

a scan-insertion system for receiving an HDL description of an integrated circuit design and for generating a scannable netlist based on said HDL description, wherein said scan-insertion system inserts a scan chain of scan cells in said integrated circuit design;

a scan chain partitioning system for partitioning said scan chain into a plurality of sets of re-orderable scan cells and for reporting partitioning information indicative thereof; and

a place-and-route system for generating a layout from said scannable netlist, said place-and-route system for re-ordering said scan cells of said scan chain based on said partitioning information by re-ordering scan cells of a same set and not re-ordering scan cells of different sets.

9. The computer controlled electronic design automation system as recited in Claim 8 wherein said scan chain partitioning system forms said plurality of sets of re-orderable scan cells by grouping scan cells of said scan chain into different sets according to their respective clock domains.

10. The computer controlled electronic design automation system as recited in Claim 8 wherein said scan chain partitioning system forms said plurality of sets of re-orderable scan cells by grouping scan cells of said scan chain according to their respective edge-sensitivity types.

11. The computer controlled electronic design automation system as recited in Claim 8 wherein said scan chain partitioning system forms said plurality of sets of re-orderable scan cells by grouping scan cells of said scan chain according to their respective positions with respect to a reconfigurable multiplexer.

12. The computer controlled electronic design automation system as recited in Claim 8 wherein said scan chain partitioning system forms said plurality of sets of re-orderable scan cells by grouping scan cells of said scan chain based on their respective clock skew tolerance levels.

13. The computer controlled electronic design automation system as recited in Claim 8 wherein said scan chain partitioning system forms said plurality of sets of re-orderable scan cells by grouping scan cells of said scan chain based on their respective surrounding cone logic.

14. The computer controlled electronic design automation system as recited in Claim 8 wherein said scan chain partitioning system forms said plurality of sets of re-orderable scan cells by grouping scan cells of said scan chain according to their output switching times.

15. A computer system comprising:

a processor coupled to a bus; and

a computer readable memory unit coupled to said bus, said memory unit having a program stored therein causing said computer system to perform an electronic design automation process, said process comprising the steps of:

(a) receiving a scannable netlist of an integrated circuit design, said scannable netlist comprising a scan chain having serially ordered scan cells;

(b) partitioning scan chain into a plurality of sets of re-orderable scan cells and generating partitioning information indicative thereof;

(c) providing said scannable netlist and said partitioning information to a layout process; and

(d) said layout process re-ordering said scan cells of said scan chain based on said partitioning information by only re-ordering scan cells of a same set and not reordering scan cells of different sets.

16. The computer system as recited in Claim 15 wherein said step (b) of said process further comprises the step of grouping scan cells of said scan chain into different sets based on their respective clock domains.

17. The computer system as recited in Claim 15 wherein said step (b) of said process further comprises the step of grouping scan cells of said scan chain into different sets based on their respective edge sensitivity types.

18. The computer system as recited in Claim 15 wherein said step (b) of said process further comprises the step of grouping scan cells of said scan chain into different sets based on their respective positions in relation to a reconfigurable multiplexer of said scan chain.

19. The computer system as recited in Claim 15 wherein said step (b) of said process further comprises the step of grouping scan cells of said scan chain into different sets based on their respective clock skew tolerance levels.

20. The computer system as recited in Claim 15 wherein said step (b) of said process further comprises the step of grouping scan cells of said scan chain into different sets based on their respective surrounding cone logic.

21. The computer system as recited in Claim 15 wherein said step (b) of said process further comprises the step of grouping scan cells of said scan chain into different sets based on their respective output switching times.

22. A method of constructing a scan chain comprising the steps of:

a) adding scan cells to a netlist description of an integrated circuit design, said scan cells being coupled serially together to form a first scan chain having a scan cell ordering;

b) partitioning said scan cells of said first scan chain into sets of scan cells and generating partitioning information indicative thereof, said step b) comprising the steps of:

b1) partitioning said scan cells of said first scan chain into sets according to the clock domain of said scan cells wherein scan cells of a given set share the same clock domain; and

b2) partitioning scan cells of said sets of step b1) into subsets according to edge sensitivity of said scan cells wherein scan cells of a given subset share the same edge sensitivity and the same clock domain; and

c) constructing a second scan chain by breaking said scan cell ordering of said first scan chain and reordering said scan cells based on said partitioning information wherein only scan cells of a same set are allowed to be reordered.

23. The method as described in Claim 22 wherein said step c) is performed during placing and routing processes performed on said netlist description.

24. The method as described in Claim 23 wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the relative positions of said scan cells to a reconfigurable multiplexer of said first scan chain wherein scan cells of a given subset share

the same edge sensitivity, the same clock domain and the same relative position to said reconfigurable multiplexer.

25. The method as described in Claim 23 wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the respective surrounding cone logic of said scan chains wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same surrounding cone logic.

26. The method as described in Claim 23 wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the respective switching times of said scan chains wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same power rail.